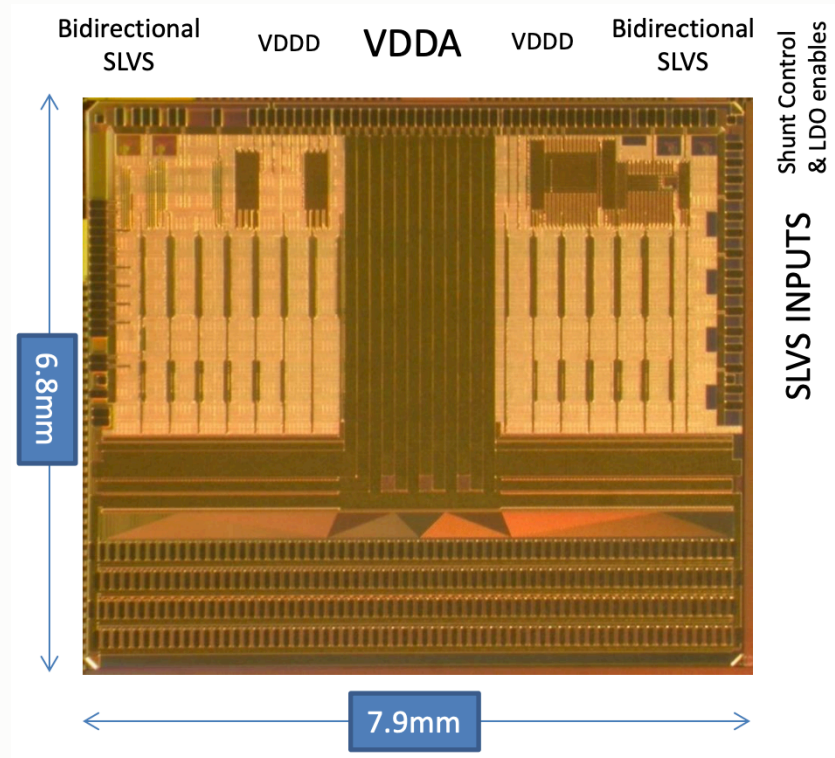


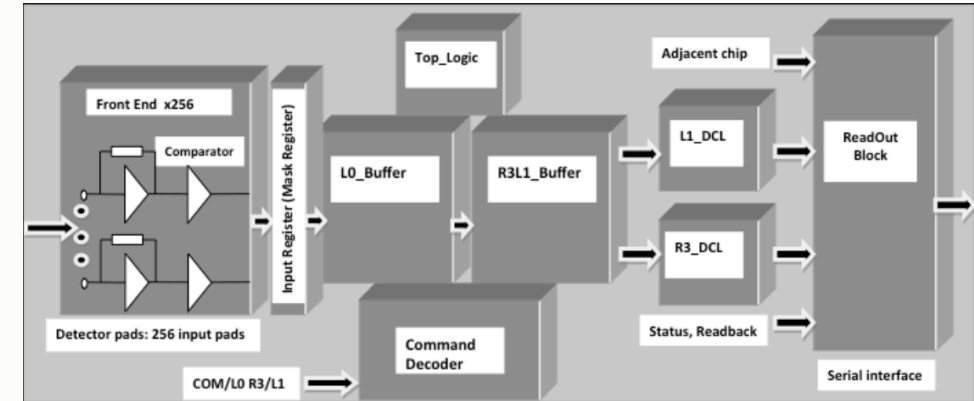
SpiceBind: Bringing SPICE into RTL Verification

Tomasz Hemperek

ABC130: A strip readout ASIC for CERN



Source: ACES 2014



Source: CERN CDS

- Large mixed-signal ASIC for ATLAS at LHC
- 256-channel analog front-end plus a large digital section
- Design reviews and a full verification campaign

First silicon: no data on output

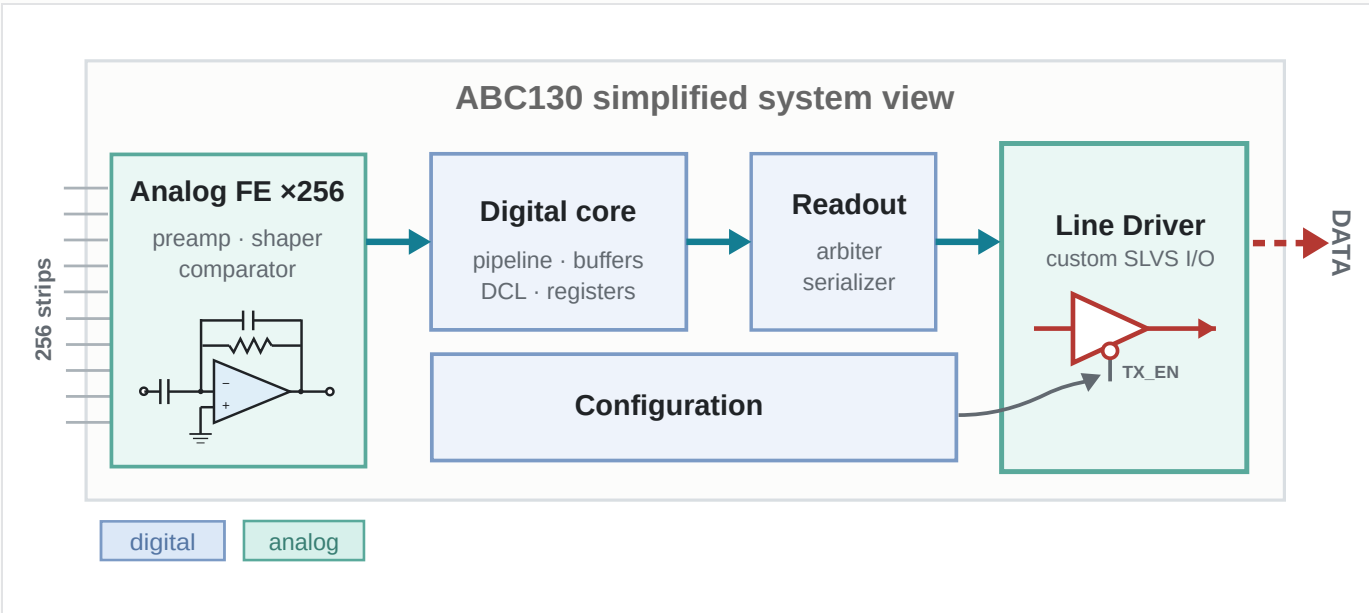
What went wrong?

Failure symptom

No data output. The custom SLVS transceiver and its functional Verilog model disagreed on the polarity of the direction signal.

Reviews and tests were not enough

They still missed a **mismatch between the functional model and the actual circuit.**

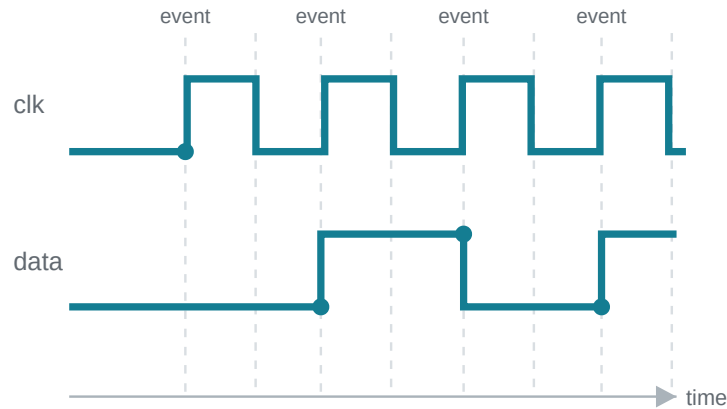


How do we catch bugs like this?

- Check the analog/digital boundary, and each side on its own.
- Drive the real custom circuit from the existing digital testbench.
- **Replace only the blocks that need circuit-level accuracy.**

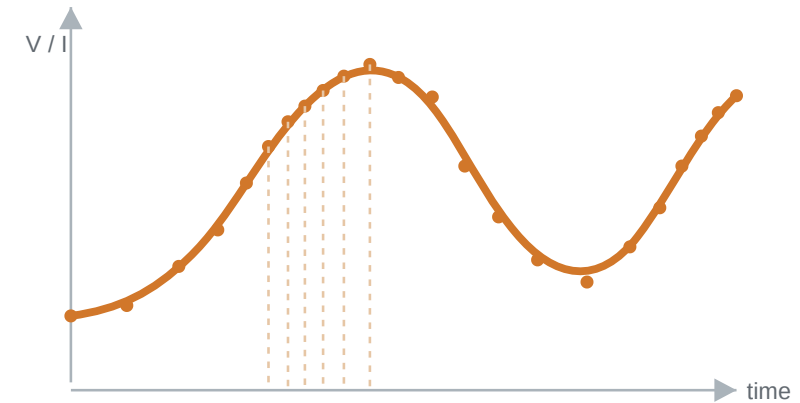
Digital vs. analog simulation

Digital



- Discrete logic states (0, 1, X, Z)
- Event-driven: jump to the next event
- Scales to large systems and long simulations

Analog / SPICE



- Continuous-valued voltages and currents
- Adaptive timesteps and nonlinear circuit equations
- Transistor-level accuracy, but slow to run

Mixed-signal designs need both. Behavioral models keep system simulation fast, but they can disagree with the actual circuit.

Open-source mixed-signal approaches

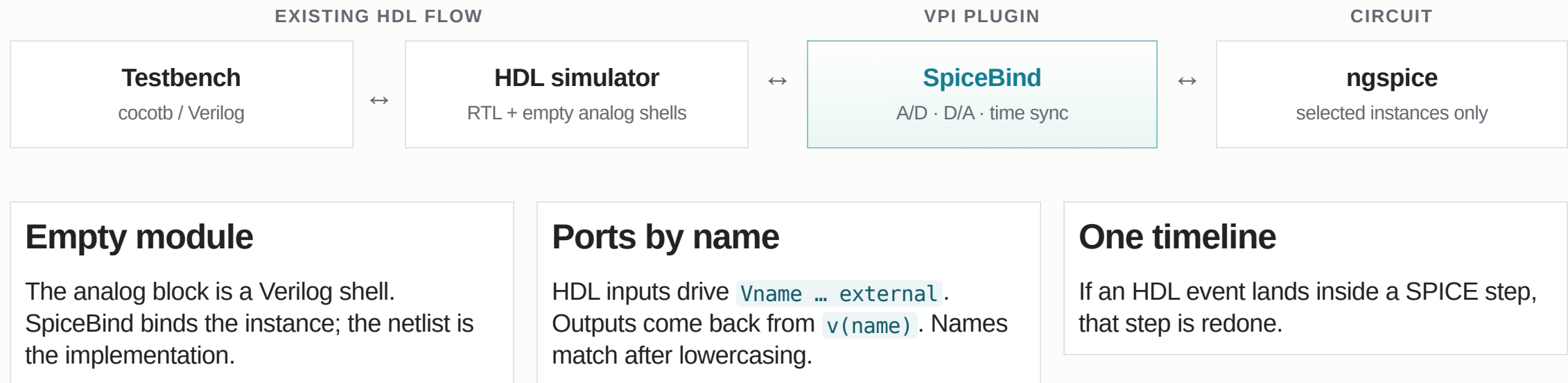
Approach	Top level	Digital execution	What it does
SpiceBind	HDL simulator	Normal HDL simulation	Selected HDL instances are replaced by SPICE.
ngspice d_cosim	ngspice / XSPICE	HDL compiled as an XSPICE model	SPICE-first flow: HDL blocks live inside ngspice.
Yosys → XSPICE	ngspice / XSPICE	RTL mapped to gates and storage elements	Single runtime simulator; digital behavior is synthesized logic.
cocotbext-ams	cocotb / Python	Normal HDL simulator	Python coordinates HDL and analog simulators such as ngspice or Xyce.

SpiceBind is HDL-first: keep the digital verification environment and use circuit-level simulation only for selected blocks.

* Commercial Verilog-AMS and real-number-modeling flows are not compared here.

SpiceBind

Keep the digital simulator as the top level. Attach ngspice only to the blocks that need a real circuit.



Where SpiceBind helps

Existing HDL flow

Keep the same RTL, testbench, cocotb, waveform viewers, and regressions.

SPICE only for analog blocks

Run SPICE only for the instances where the circuit changes what the system does.

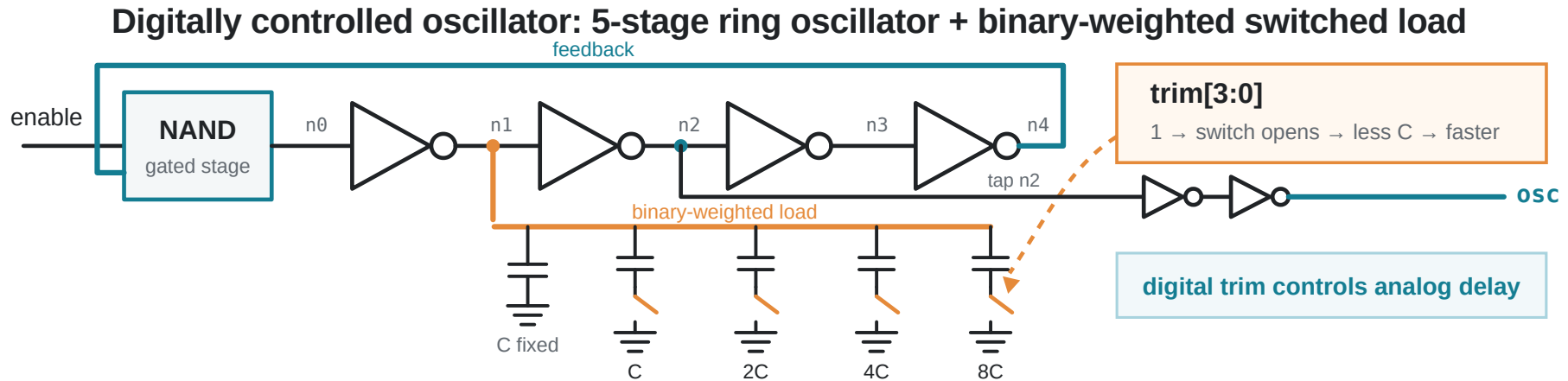
Mixed-signal checks

Write tests and sweeps for ADCs, PLLs, DCOs, sensor front-ends, bias loops, and custom I/O.

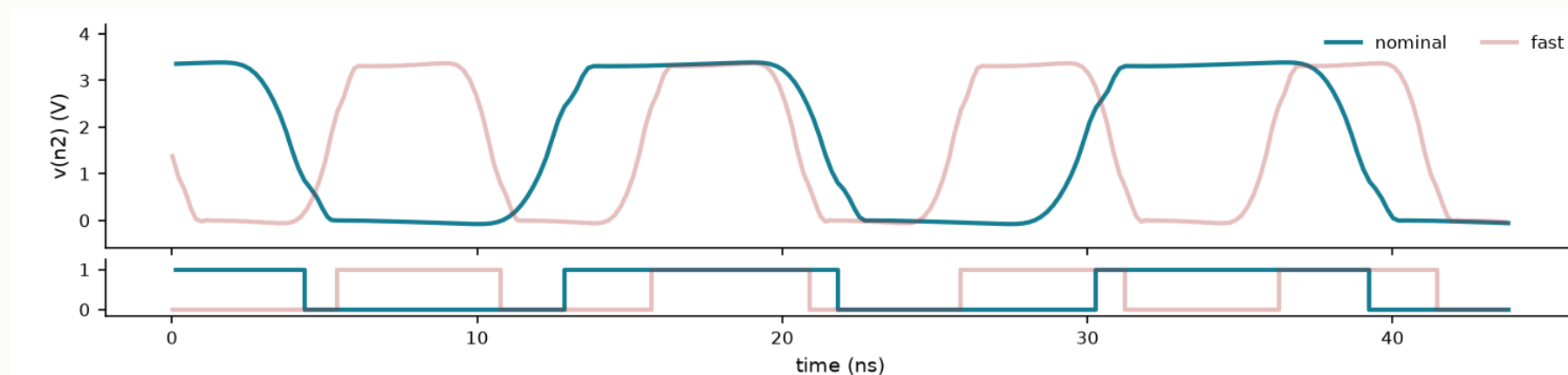
Open-source stack

Icarus Verilog, Verilator, ngspice, cocotb. Standard VPI, BSD-3-Clause. Works without a vendor AMS simulator.

Example: DCO calibration

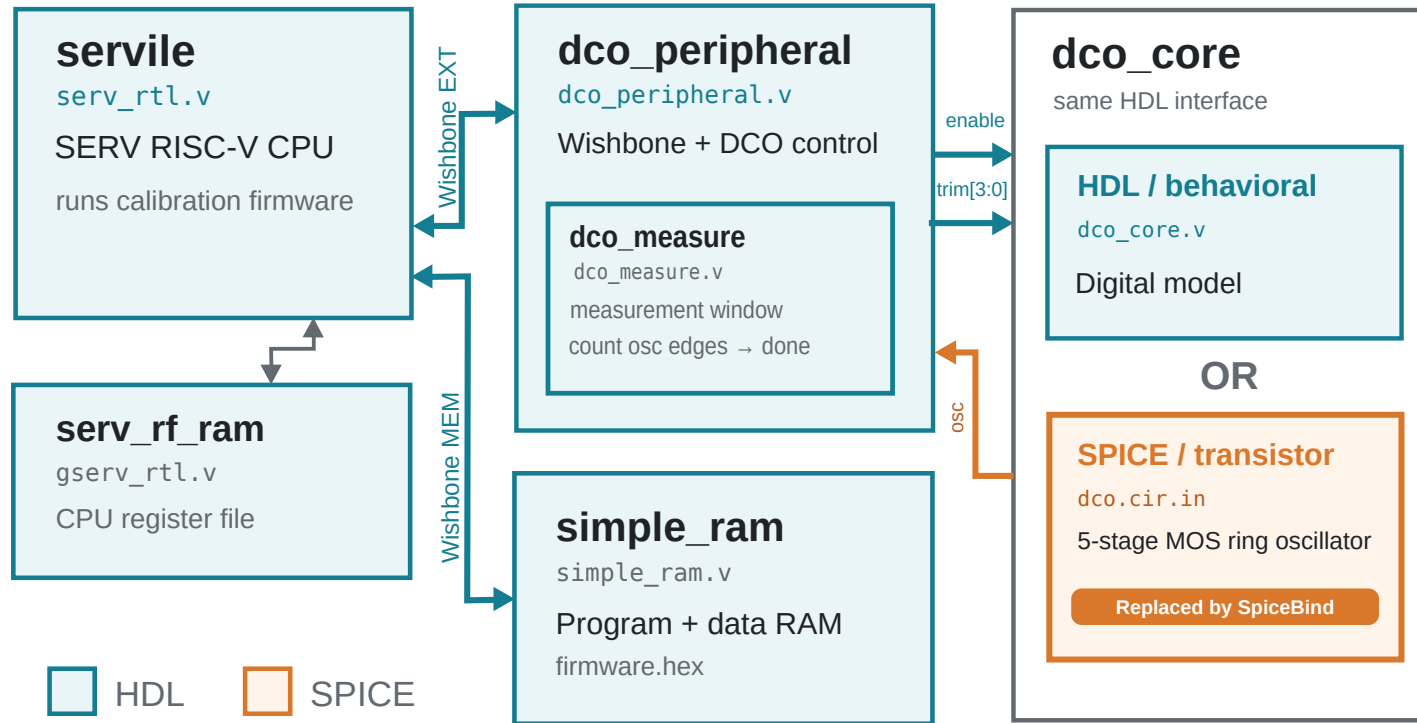


Analog oscillation simulation for nominal and fast corners



Same RTL system, one replaceable block

top.v top-level RTL integration



Same digital system

SERV CPU, RAM, Wishbone, and measurement logic stay RTL. The firmware runs unchanged.

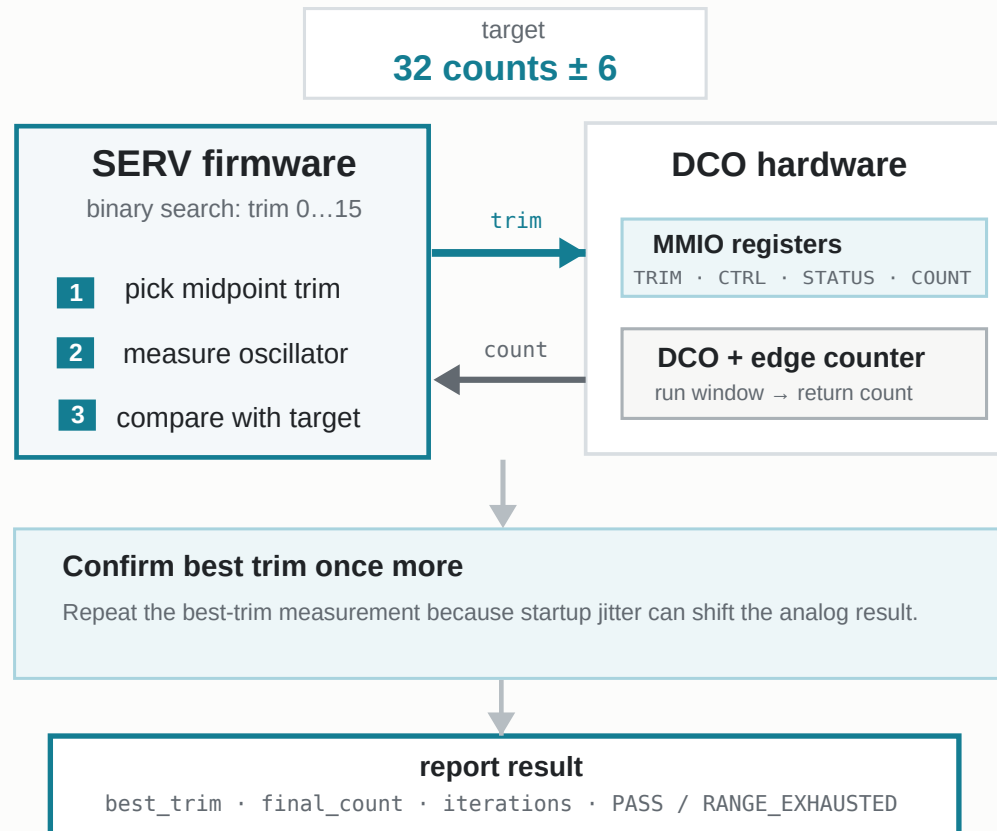
One replaceable block

`dco_core` keeps the same HDL interface: `enable`, `trim[3:0]`, `osc`. Use the behavioral model for fast runs or bind the SPICE circuit with SpiceBind.

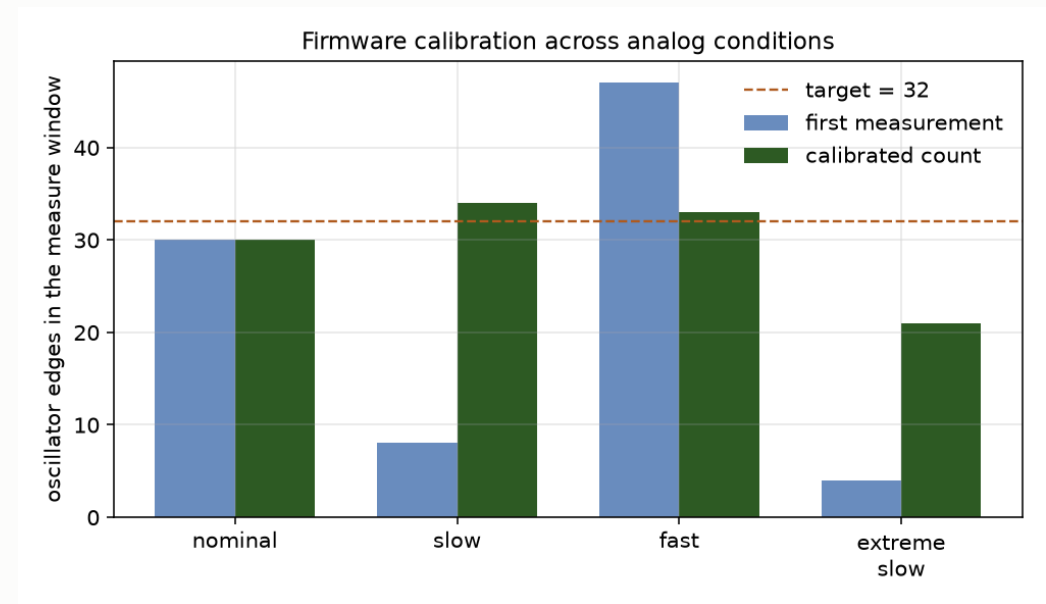
Firmware, RTL and testbench stay unchanged. Only the DCO implementation is replaced.

Firmware calibrates the circuit across corners

Firmware calibration loop



Results before and after trimming across corners



Behavioral



~1 s

SPICE



~50 s

* Generic BSIM3 demo models, not a foundry PDK; extracted PDK netlists can be much slower.

SpiceBind: practical mixed-signal verification



SpiceBind adds circuit-level simulation to selected blocks in an RTL verification flow.

Same RTL flow

- Keep the digital simulator as the top level.
- Empty Verilog shell; bind one instance to ngspice.
- Same testbench and firmware; compare behavioral and SPICE runs.

Before silicon

- Catch model/circuit mismatches before tape-out.
- Debug mixed-signal behavior in regression.
- Spend SPICE only on the blocks that need it.

Icarus, Verilator, VPI

- Tested with Icarus Verilog and Verilator.
- The plugin is standard VPI.
- Other VPI-capable simulators should work; they are not qualified yet.

Early release. Feedback and contributions are welcome.

 **themperek/spicebind**

 [linkedin.com/in/hemperek](https://www.linkedin.com/in/hemperek)

Thanks to

DECTRIS